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Result # 1    Relevance:

**Dispatcher Queue to Provide Processor Affinity in a Multiprocessor**

1994-02-01

IPCOM000111232D

English

Disclosed is an efficient scheme for dispatcher queue management and process selective implement affinity-based scheduling in a multiprocessor, where the term affinity-based refers to running a process on a processor that ran this process previously so that the .

Result # 2    Relevance:

**Task Scheduling on a Multilevel Multiprocessor**

1983-11-01

IPCOM000047393D

English

A multilevel processor is a processor in which independent processing of tasks is possible plurality of priority levels, current processing taking place at the most significant level at least one pending task exists. A task queue is maintained at each ...

Result # 3    Relevance:

**Serial Resource Managing**

1977-05-01

IPCOM000088196D

English

A programmed processor for controlling a subsystem, such as a magnetic storage subsystem printing subsystem having a plurality of assignable printers, often requires immediate attention to certain resources on a time-varying basis. Generally, most ...

Result # 4    Relevance:

**Parallel Execution of Non-Uniform Component-Based Dependency-Driven Workloads**

2003-10-17

IPCOM000020019D

English

Disclosed is a system that executes a componentized, non-uniform, dependency-based parallel. A componentized, non-uniform, dependency-based workload is a workload conforming following attributes: comprised of logical units of work (componentized); logical ...

Result # 5    Relevance:

**Task Scheduling Algorithm for a Teleprocessing Communications Controller**

1974-03-01

IPCOM000081018D

English

This description presents a task scheduling algorithm such that, when it is integrated with management algorithm described in the publication entitled "Dynamic Storage Manager Teleprocessing Communications Controller", IBM Technical Disclosure ...

Result # 6    Relevance:

**Dynamic Program Priority in Multi-Tasking Systems**

1986-08-01

IPCOM000061549D

English


Dynamic Program Priority (DPP) varies a task's priority based on task behavior and system provide the following functions: A user can assign fixed or variable priorities. Each system priority has a base value. Variable priority may vary above or below ...

Result # 7    Relevance:

**Off-Level Interrupt Handling**

1991-02-01 IPCOM000119727D English  
A program is disclosed that provides a mechanism where the processing of long hardware interrupt service routines do not adversely affect the overall system integrity and the other I/O devices. This is accomplished by splitting the interrupt service ...

---

Result # 8 Relevance: 

### **Preemptive Background Scheduling**

1991-01-01 IPCOM000119218D English  
Disclosed is an algorithm that permits a round robin, run to completion task scheduling alter task scheduling without relying on: - Dedicated microprocessors and/or control circuitry to manage critical time-driven events. - System level knowledge in ...

---

Result # 9 Relevance: 

### **Integrated Operating System Scheduler**

1979-02-01 IPCOM000066202D English  
Described is a SCHEDULER PROCESS decomposition and implementation for a multiprocessor operating system using multiple-level interrupt controller hardware. The resulting system hardware and software functions to achieve a system which (1) is completely ...

---

Result # 10 Relevance: 

### **Dynamic Bubbling Task Dispatching Algorithm**

1970-06-01 IPCOM000072289D English  
A method of running a multiprogramming system is to dynamically determine the I/O boundedness of the tasks to be dispatched and to give higher priority service to the one that performs the most I/O. A group of tasks which is heuristically dispatched is identified as ...

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**Search query:** A process scheduling apparatus has a delayed task handling process for processing tasks having variable priorities and multiple other processes for handling processed delayed tasks. Fixed priorities are assigned to the other processes. The process sequentially executes the delayed task handling process and the other processes assigned priorities. A delayed task registration processor stores newly generated tasks with assigned priorities in a queuing table. A delayed task priority controller selects a task with the highest priority in the queuing table. A process priority controller transfers the delayed task handling process to the same priority as the priority of the task.

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Result # 1      Relevance:

**Priority Scheduling Algorithm**

1989-05-01

IPCOM000034988D

English

This scheduling algorithm is based on priority level and arrival time. Higher priority requests are serviced before lower priority requests which have not yet aged sufficiently. When a low priority request has aged sufficiently, it will be serviced and cannot be ...

Result # 2      Relevance:

**Round Robin of Equal Priority Initiators**

1973-02-01

IPCOM000078638D

English

When more than one initiator has the same dispatching priority, they do not get equal service. They are dispatched due to their order on the TCB (Task Control Block) queue.

Result # 3      Relevance:

**Dynamic Bubbling Task Dispatching Algorithm**

1970-06-01

IPCOM000072289D

English

A method of running a multiprogramming system is to dynamically determine the I/O of each task and the boundedness of the tasks to be dispatched and to give higher priority service to the one with the most I/O. A group of tasks which is heuristically dispatched is identified as ...

Result # 4      Relevance:

**Serial Resource Control Technique for Priority Pre-Emptive Tasking**

1971-08-01

IPCOM000075119D

English

A common problem existing in multiprogramming environments is the controlled sharing of a reusable resource, (SRR) by the operating system. Requests for SRR ownership must be in a strict priority sequence. Two conditions exist: Simultaneous access to an ...

Result # 5      Relevance:

**Prevention of Low Priority Lockout**

1987-02-01

IPCOM000040857D

English

Normally, interrupt and priority of tasks are ordered from a high priority to a low priority and results in servicing the most critical tasks with the highest priority first while other low priority tasks await completion of the higher priority tasks. In some ...

Result # 6      Relevance:

**Maximum Response Time Control**

1972-01-01

IPCOM000076045D

English

An expanded table driven task scheduling algorithm is provided, which allows for a change in priority for a given user if a predefined time limit is exceeded. This permits a task which is given low priority under normal loading conditions to be assured of ...

Result # 7      Relevance:

**Improved Performance of Priority Dispatcher**

1976-07-01

IPCOM000086124D

English

A multitask dispatcher's main function is to select and give control to the highest priority task. However, if a high-priority task requires the use of a resource such as the transier is owned by a lower priority task, then it must wait until the ...

---

Result # 8      Relevance: 

**Virtual Machine Group Control System Dispatching Program**

1985-03-01

IPCOM000063466D

English

A data structure for dispatching and scheduling tasks is formed by combining multiple c linked lists that are interconnected by a linear doubly-linked list. This structure is referred "cylindrical queue". The Group Control System (GCS) ...

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
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English

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## Patents

Patents 1 - 10 on **setting priority of a delayed process**. (0.51 seconds)[Data processing device having](#)[Sort by relevance](#) | [Sort by date \(new first\)](#) | [Sort by date \(old first\)](#)[improved interrupt controller to process ...](#)

US Pat. 5659759 - Filed Nov 4, 1996 - Kabushiki Kaisha Toshiba

This results in the drawback whereby the **priority** 65 15 executes interrupt **process** starting procedures which ranking order mechanism of the interrupt ...[Delay distortion suppressing system for ATM communication system](#)

US Pat. 5301193 - Filed Nov 14, 1991 - Fujitsu Limited

The timing pulse TP for **setting** the cell transmission time ST is shown in (e) of ... 164. **delayed** by the delay circuit 217 until the read address is Next, ...[Apparatus and method for message queuing in a database system](#)

US Pat. 6058389 - Filed Oct 31, 1997 - Oracle Corporation

4A, in step 400 the **process** tests whether the Sequence Deviation value is ...The Delay value 234f of message 238 is 10 and its **Priority** value 236f is 80. ...[Bus access control for a multi-host system using successively decremented ...](#)

US Pat. 4972313 - Filed Aug 7, 1989 - Bull HN Information Systems Inc.

When the loop until it is the highest **priority** host having a Delay bus becomes available, the **process** proceeds to Step 50, Count of zero and may proceed to ...[Content-aware web switch without \*\*delayed\*\* binding and methods thereof](#)

US Pat. 6772211 - Filed Apr 30, 2002 - Transtech Networks USA, Inc.

Step 614: Set the packet to a default **priority**. Go to Step 630. ... **process** does not need to "wait" (hence requiring **delayed** binding) for application layer ...[Methods and apparatus for random chip delay access \*\*priority\*\* in a ...](#)

US Pat. 6674765 - Filed Oct 14, 1998 - Lucent Technologies Inc.

The method of claim 1, wherein the preestablished access **priority** classes ... further wherein the remote terminal performs a backoff **process** when the access ...[Method and apparatus for performing \*\*priority\*\* control for cells in output ...](#)

US Pat. 5550823 - Filed Apr 28, 1995 - NEC Corporation

A read **process** in the read controller 23 will be described below with ... 6 explains transition related to the **priority** class of each logical queue 22. ...[Storage control apparatus](#)

US Pat. 6904469 - Filed Aug 31, 2001 - Hitachi, Ltd.

The delay **setting** value 517 is not changed and the I/O **process** continues. Even if the I/O processing of the **priority** channel port ...[Communication system and communication method](#)

US Pat. 5699521 - Filed Mar 22, 1995 - Hitachi, Ltd.

In particular, the communication system having a plurality of terminals connected account **setting a priority process** level depending on ...

Segmented memory transfer and message **priority** on synchronous/asynchronous ...

US Pat. 5214774 - Filed Jul 30, 1990 - Motorola, Inc.

One additional master's, at 1113, and if so, acknowledgement **process-** delay occurs during ... by **setting** its SLAV-REQ bit and from being in the queue at ...

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